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CLAIMS

[Claim(s)]
[Claim 1] A slot is alternatively formed in the surface layer of the first principal plane of the first electric conduction form semi-conductor substrate. It is what constitutes MOSFET of the trench structure where a source electrode is formed on the first principal plane surrounded in this slot, a gate electrode is formed through an insulator layer on the front face of this slot, and a drain electrode is formed on the second principal plane. The power semiconductor device characterized by for a source electrode contacting the first electric conduction form semi-conductor substrate front face except said slot, and forming a gate electrode by the second electric conduction form semi-conductor film.
[Claim 2] A slot is alternatively formed in the surface layer of the first principal plane of the first electric conduction form semi-conductor substrate. It is what constitutes MOSFET of the trench structure where a source electrode is formed on the first principal plane surrounded in this slot, a gate electrode is formed through an insulator layer on the front face of this slot, and a drain electrode is formed on the second principal plane. A source electrode contacts the first electric conduction form semi-conductor substrate front face except said slot, and a gate electrode is formed with a metal. The power semiconductor device characterized by forming a gate electrode with the metal with which phi m>=chi+Eg / 2q is filled when forbidden-band width of face of the semi-conductor which forms chi and a substrate for the electron affinity of the semi-conductor which forms phim and a substrate for the work function of this metal is made into Eg/q (Eg:band GYAPU, q: charge).
[Claim 3] The power semiconductor device according to claim 2 characterized by using a gate electrode as nickel (nickel) or platinum (Pt) when the first electric conduction form semi-conductor substrate is used as silicon.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention is low on resistance and relates to the power semiconductor device of the vertical mold which has trench gate structure.
[0002]
[Description of the Prior Art] According to the application, various structures are applied to the power semiconductor device. Drawing 6 is the vertical mold MOSFET of the trench structure of having low on resistance currently manufactured conventionally. It is n+ to the semi-conductor substrate 1 of n form. The drain field 7, n drift region 6a, the p base region 14, and n+ The source field 4 is formed and gate electrode 2b by which the impurity atom of n form was doped through gate dielectric film 3 is formed on the gate slot 13. The source electrode 8 is n+. It is in contact with the source field 4 and the p base region 14. This structure raises the consistency of a unit cell and has the advantage which can make on resistance small. The power semiconductor device of an insulated-gate drive of the structure which does not include any pn junction shown in drawing 7 is proposed in order to lower on resistance furthermore. In drawing 7 , the gate slot 13 is formed in the surface layer of one principal plane of the semi-conductor substrate 1 of n form, and gate electrode 2b is formed through gate dielectric film 3 on the front face of this gate slot 13. It is n+ to the surface layer of the semi-conductor substrate 1 surrounded by this gate slot 13. The source field 4 is formed and it is n+. The source electrode 8 is formed on the source field 4. The field surrounded by the gate slot 13 with the semi-conductor substrate 1 turns into the 1st drift region 5 of n form, and the field under it turns into the 2nd drift region 6 of n form. It is n+ to the surface layer of the principal plane of another side of the semi-conductor substrate 1. The drain field 7 is formed and it is n+. The drain electrode 10 is formed on the drain field 7. Gate electrode 2b is formed by the polish recon of n form.
[0003] Since an accumulation layer is formed in the field which counters with gate electrode 2b of the 1st drift region 5 at the time of ON and this accumulation layer serves as a channel unlike the component of structure conventionally which is shown in drawing 6 , the component of the structure of drawing 7 can reduce channel resistance sharply. Moreover, since there is no are recording of the carrier by pn junction, compaction of the switching time can be performed, since there is no pn junction, and current concentration does not take place, it has the advantage which can improve the destructive tolerated dose of a component.
[0004] Moreover, although the component of drawing 6 and drawing 7 is a power semiconductor device of an insulated-gate drive mold, in order to use the polish recon of n form and to lower electric resistance, high concentration doping of the gate electrode 2b is carried out. Moreover, polish recon is made to a high grade, bears an elevated temperature further, is easy to process it and is used widely.
[0005]
[Problem(s) to be Solved by the Invention] If gate voltage 2b will be impressed [electrode] to the 1st drift region 5 and the 2nd drift region 6 through gate dielectric film 3 in negative and a source electrode if bias of the gate electrode is just carried out, a depletion layer 11 will spread to these fields, if the

actuation at the time of OFF is explained, and this depletion-layer edge 12 next sticks, the current path between the source electrode 8 and the drain electrode 10 will be severed, and a current will be intercepted. The component is turned on when, as for this, the electrical potential difference is not impressed to gate electrode 2b, as for the component of drawing 7 . The stage when the electrical potential difference has not established this in a gate drive circuit system in early stages of powering on has inconvenient [very big], when applying to the inverter that a component will be in a short circuit condition.

[0006] The purpose of this invention is in the condition of solving the aforementioned technical problem and not impressing gate voltage, and is to offer the semiconductor device for power of the insulated-gate structure which can consider the current path between source drains as high resistance, or can intercept this current path.

[0007]

[Means for Solving the Problem] In order to attain said purpose, a slot is alternatively formed in the surface layer of the first principal plane of the first electric conduction form semi-conductor substrate. It is what constitutes MOSFET of the trench structure where a source electrode is formed on the first principal plane surrounded in this slot, a gate electrode is formed through an insulator layer on the front face of this slot, and a drain electrode is formed on the second principal plane. A source electrode contacts the first electric conduction form semi-conductor substrate front face except said slot, and considers as the configuration in which a gate electrode is formed by the second electric conduction form semi-conductor film.

[0008] Moreover, a slot is alternatively formed in the surface layer of the first principal plane of the first electric conduction form semi-conductor substrate. It is what constitutes MOSFET of the trench structure where a source electrode is formed on the first principal plane surrounded in this slot, a gate electrode is formed through an insulator layer on the front face of this slot, and a drain electrode is formed on the second principal plane. A source electrode contacts the first electric conduction form semi-conductor substrate front face except said slot, and a gate electrode is formed with a metal. When forbidden-band width of face of the semi-conductor which forms chi and a substrate for the electron affinity of the semi-conductor which forms phim and a substrate for the work function of this metal is made into Eg/q (Eg: an energy gap, q:charge), it is good to form a gate electrode with the metal with which phi m>=chi+Eg / 2q is filled. When the aforementioned first electric conduction form semi-conductor substrate is used as silicon, it is good to use a gate electrode as nickel (nickel) or platinum (Pt).

[0009] By providing this means, the depletion layer from right and left can be stuck by a depletion layer spreading directly under gate dielectric film, even when gate bias is zero, and enlarging the impedance of a component, and carrying out micro processing of the unit cell, and a current path can be intercepted.

[0010]

[Embodiment of the Invention] Drawing 1 is the important section sectional view of the component of the 1st example of this invention. Each field stated to the semi-conductor substrate 1 below is formed. n+ On the drain field 7, the laminating of the 2nd drift region 6 and the 1st drift region 5 is carried out, and it is n+ on the 1st drift region 5. The source field 4 is formed and it is n+. The source electrode 8 is formed on the source field 4. Moreover, gate dielectric film 3 is formed in the front face of the gate slot 13, and the gate electrode 2 is formed so that the gate slot 13 may be filled on gate dielectric film 3. This gate electrode 2 is formed by the polish recon which doped the impurity atom of p form. Therefore, also in the condition that gate voltage is not impressed to the 1st drift region 5 and the 2nd drift region 6 of n form, a depletion layer 11 spreads and the impedance of narrowing and this part increases [the current path 35] so that it may mention later. A unit cell is further made detailed, if the width of face W of the 1st drift region 5 is narrowed, elongation L of a depletion-layer edge will become large, the depletion-layer edge 12 from right and left is stuck, the current path 35 is closed and a current serves as a component of the no MARIOFU mold of being intercepted. In addition, n+ The drain electrode 10 is formed in drain field 7 front face.

[0011] Drawing 2 is drawing explaining the concept of this invention, and, as for this drawing (a), the gate electrode of an energy band Fig. in case a gate electrode is the polish recon of n form, and this drawing (b) is an energy band Fig. in the case of being the polish recon of p form. Both drawings are n forms and the semi-conductor substrate 23 is the case where gate bias is zero. In this drawing (a), there is no deflection of an energy band, therefore a depletion layer does not spread in the semi-conductor substrate 23. In this drawing (b), if the gate electrode 2 is formed by the polish recon of p form and it is high concentration, as shown in drawing, it will turn at the energy band of the semi-conductor substrate 23. Therefore, the crooked part serves as a depletion layer 11. If this depletion layer 11 spreads, the impedance of a component will become large, and a current path will be intercepted when it spreads further. The deflection of this energy band becomes the case where the negative electrical potential difference of -1.2V which are a band gap is impressed to gate electrode 2b of n form, and equivalence.
[0012] Drawing 3 is the current and the voltage characteristic between the source drains at the time of impressing negative bias to the gate electrode of n form. The component made as an experiment has the gate electrode of n form, and the width of face W of the 1st drift region is 5 micrometers. One quadrant is the forward direction forward and source negative in a drain in the case where gate voltage is impressed at 1V step from 0 to -10V, and three quadrants are hard flow. In the forward direction, if the electrical potential difference VDS between the drain sources is read by 4V when gate voltage is set to 0V and -1V, the current IDS between the drain sources will be set to 10A and 3A, and, in the case of -1V, an impedance will become large about 3 times to 0V. The current IDS between the drain sources serves as zero and a current path is intercepted to make gate voltage lower than -3V. If it is the gate electrode of p form like the configuration of drawing 1 , even when not impressing gate voltage, the depletion layer 11 which becomes equivalent to the time of impressing gate voltage -1.2V is formed in the 1st drift region 5. This becomes equivalent to having impressed gate voltage -1.2V by drawing 3 , and comes to have a big impedance. Furthermore, in drawing 1 , if a unit cell is made detailed and the width of face W of the 1st drift region 5 is narrowed, even if the depletion-layer edge 12 sticks and it does not impress gate voltage, the current path 35 will close and it will become the component of a no MARIOFU mold.
[0013] Drawing 4 is the important section sectional view of the component of the 2nd example of this invention. Differing from drawing 1 is the point which formed gate electrode 2a with the metal which fills a degree type.
[0014]
[Equation 1] phim>=chi+Eg/2q .... (1)
[phim: -- a metaled work function, the electron affinity of chi:semi-conductor substrate, the band gap of Eg:semi-conductor substrate, and q:charge]
It becomes the component of a no MARIOFU mold by a depletion layer 11 spreading in the 1st drift region 5 and the 2nd drift region 6, and the impedance of the current path 35 increasing like the 1st example, and making a unit cell detailed further also in the condition of not impressing gate voltage to the 1st drift region 5 and the 2nd drift region 6 like the case where the polish recon of p form which is the 1st example is used by using the aforementioned metal for gate electrode 2a.
[0015] Drawing 5 is an energy band Fig. at the time of using the metal shown in a gate electrode by drawing 4 . The left-hand side of drawing shows the semi-conductor substrate 23 of n form to right-hand side on both sides of the insulator layer 22 with the metal 21 which hits a gate electrode. The energy from the vacuum level 31 to Fermi level 32 of a metal 21 is work function phim. Moreover, the energy from the vacuum level 31 to a conduction band 33 is an electron affinity chi, and the energy between a conduction band 33 and a valence band 34 is Eg/q. Although it was expressed as energy here, it is the thing of potential strictly. (1) When it is the metal 21 with which a formula is realized, as for the energy of the semi-conductor substrate 23, the deflection depletion layer 11 spreads so that it may be illustrated. Exactly, it is the same as that of the case where polish recon of p form is used as the gate electrode 2. Since a depletion layer 11 spreads in the semi-conductor substrate 23 side so that this work function phim is large, effectiveness becomes large. Since, as for Eg/q of silicon, 1.2V and an electron affinity are set to 4.05V when a semi-conductor substrate is used as silicon, the work function of the metal 21

used for gate electrode 2a is good to carry out to more than 4.65V. As a concrete metal, nickel (nickel), platinum (Pt), etc. are good. If these metals are used for a gate electrode, a depletion layer 11 comes to spread in the semi-conductor substrate 23 also at the time of zero bias, and the gate can increase the impedance of a component. Moreover, it is also possible to make a unit cell detailed, or to extend the depletion-layer edge 12 greatly by using the metal 21 of bigger work function phim for gate electrode 2a, and to intercept a current path. That is, the component of a no MARIOFU mold can be manufactured.

[0016]

[Effect of the Invention] According to this invention, the large component of the resistance between the drain sources (impedance of a component) and the component of the no MARIOFU mold which intercepts a current path can be obtained also in the time of gate zero bias by using for a gate electrode the metal with which the polish recon of p form and the aforementioned (1) formula are materialized with the electrical-potential-difference drive mold component of the trench structure where it does not have pn junction. Moreover, this component serves as very low ON state voltage in an ON state. Furthermore, if this component is applied to an inverter, a circuit does not lapse into a short circuit condition in the condition that the gate voltage of a power up is low, either, it is stabilized in the usual gate circuit, and an inverter can be operated.

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DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] The important section sectional view of the component of the 1st example of this invention
[Drawing 2] For (a), an energy band Fig. in case a gate electrode is the polish recon of n form, and (b) are [a gate electrode] an energy band Fig. in the case of being the polish recon of p form in drawing explaining the concept of this invention.
[Drawing 3] The current and voltage characteristic Fig. between the source drains at the time of impressing negative bias to the gate electrode of n form
[Drawing 4] The important section sectional view of the component of the 2nd example of this invention

[Drawing 5] The energy band Fig. at the time of using the metal shown in a gate electrode by drawing 4
[Drawing 6] The important section sectional view of the vertical mold MOSFET of the conventional trench structure
[Drawing 7] The important section sectional view of the power semiconductor device of an insulated-gate drive of the structure which does not include any conventional pn junction
[Description of Notations]
1 Semi-conductor Substrate
2 Gate Electrode
2a Gate electrode
2b Gate electrode
3 Gate Dielectric Film
4 N+ Source Field
5 1st Drift Region
6 2nd Drift Region
6a Drift region
7 N+ Drain Field
8 Source Electrode
9 Gate Electrode
10 Drain Electrode
11 Depletion Layer
12 Depletion-Layer Edge
13 Gate Slot
21 Metal
22 Insulator Layer
23 Semi-conductor Substrate
31 Vacuum Level
32 Fermi Level
33 Conduction Band
34 Valence Band

35 Current Path
L Elongation of a depletion-layer edge
W Width of face of the 1st drift region

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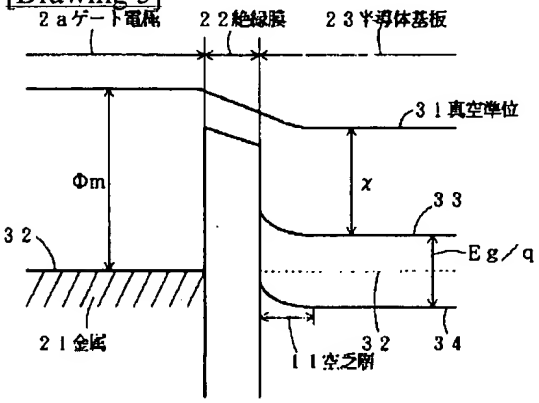
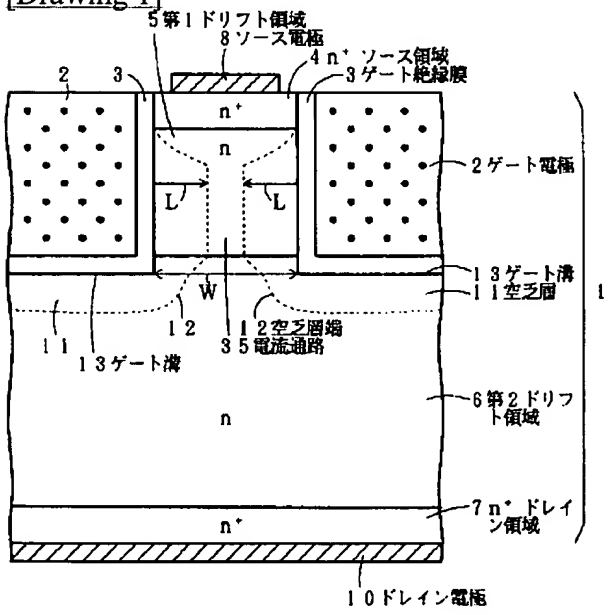
DRAWINGS

[Drawing 5]

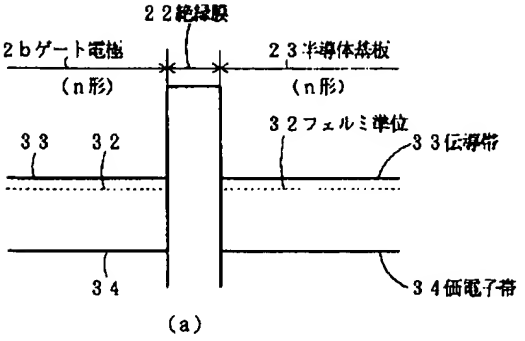


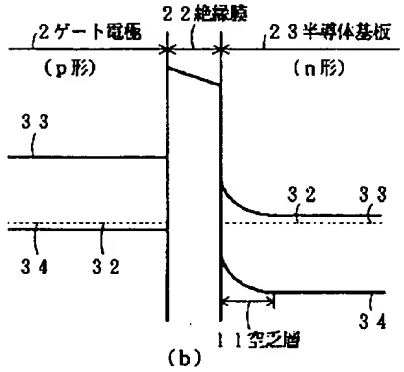
[Drawing 1]



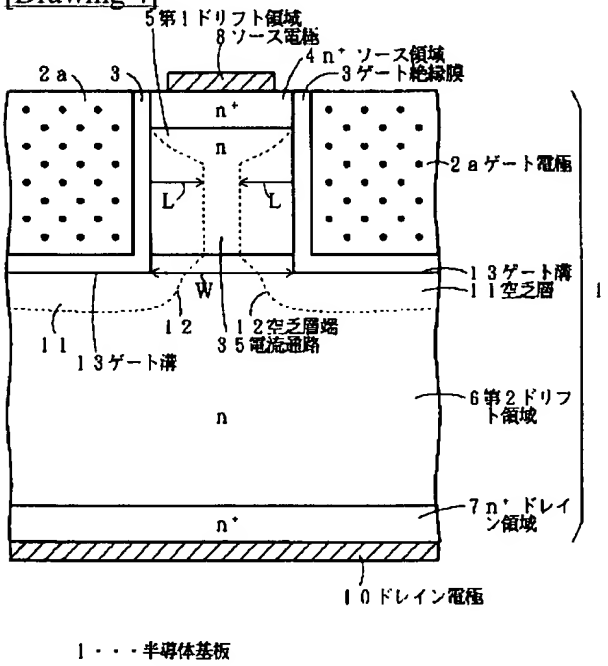
1・・・半導体基板

[Drawing 2]



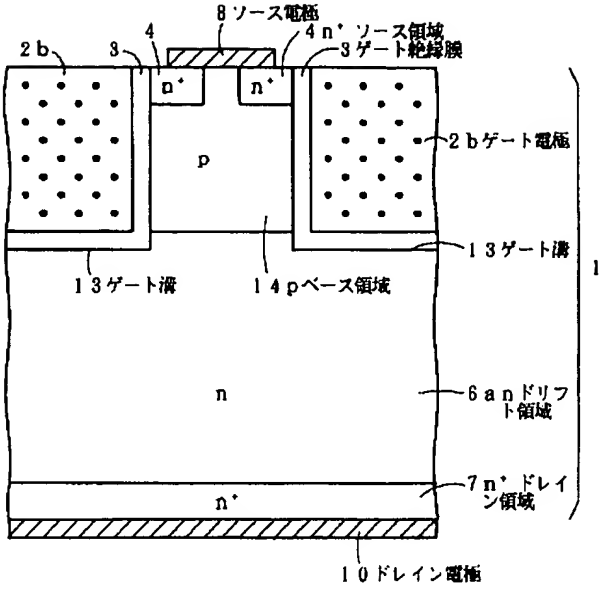


[Drawing 4]



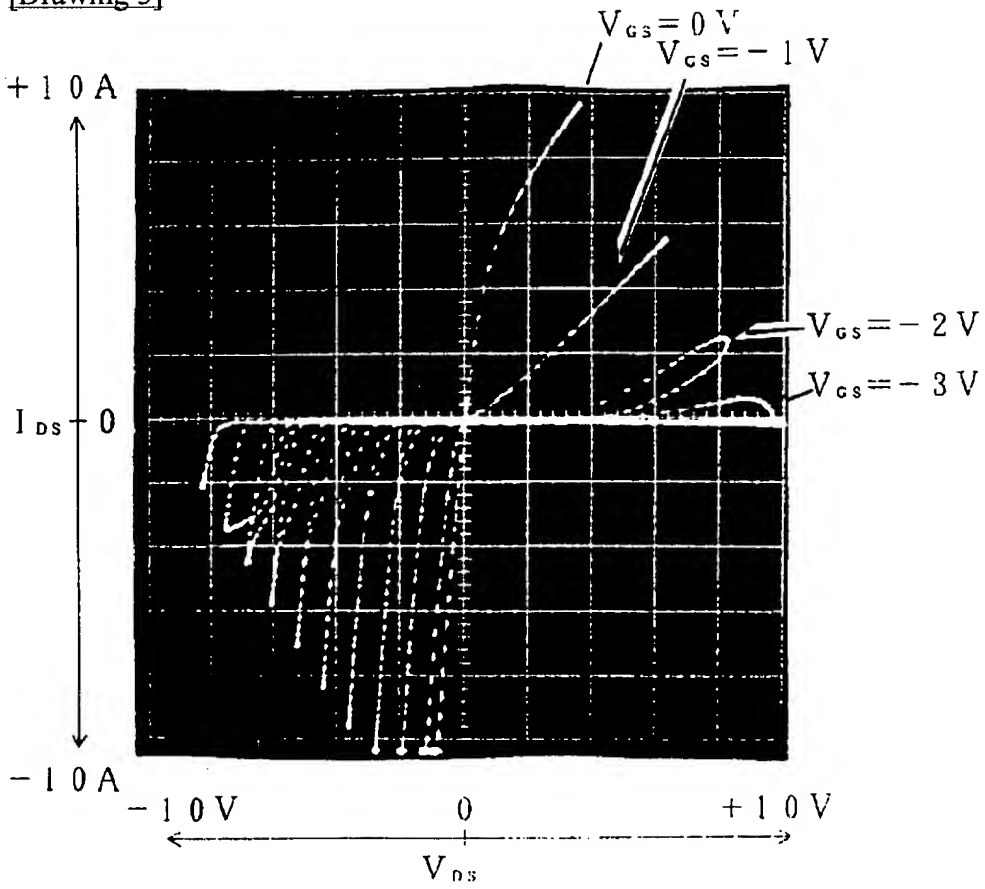
１・・・半導体基板

[Drawing 6]



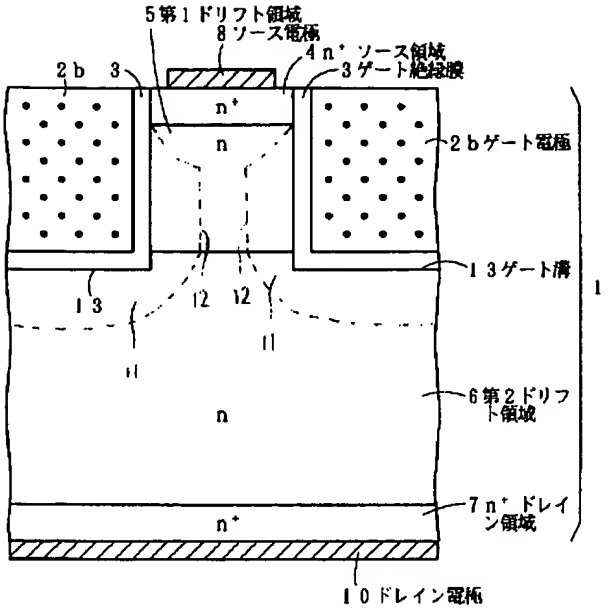
1・・・半導体基板

[Drawing 3]



V_{GS}は０Ｖから－１０Ｖまで１Ｖステップである。

[Drawing 7]



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